AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A microcomputer comprising:

an erasable and programmable non-volatile memory; and

a CPU,

wherein said CPU is capable of temporarily branching to a process ~~indicated by~~ corresponding to information ~~set to~~ in a programmable first register means for each cycle or a plurality of cycles of a unit process for the non-volatile memory, the unit process including the application of an erase voltage for an erase operation or a program voltage for a programming operation, and a verify operation~~, or every plural cycles, and said first register means is capable of programmably setting information thereto~~.

2. (Currently Amended) The microcomputer according to claim 1, wherein said CPU skips said branch process when the information ~~set to~~ in the first register means is a first set value, and branches to [[a]] the corresponding

process ~~specified based on the first set value~~ when the information is ~~except for~~ other than the first set value.

3. (Currently Amended) The microcomputer according to claim 1, further including second register means (FKEY) readable and writable by said CPU, and

wherein said non-volatile memory sets ~~the setting of~~ a second set value ~~to~~ in said second register means as a necessary condition for enabling erase and programming operations, and

said CPU sets a value other than the second set value ~~to~~ in said second register means upon said branch and ~~sets~~ resets the second set value ~~to~~ in said second register means for each return from the branch.

4. (Original) The microcomputer according to claim 3, wherein the value other than the second set value is code information indicative of the progress of an erase and program process.

5. (Currently Amended) The microcomputer according to claim 1, further including an interrupt control circuit ~~for inputting~~ that inputs an interrupt request signal

therein, and ~~performing~~ performs arbitration of interrupt requests which compete with one another, and an interrupt priority level-based interrupt mask process to thereby output an interrupt signal to said CPU, and

wherein said CPU causes said interrupt control circuit to carry out a setting for masking an interrupt lower in interrupt priority level than a non-maskable interrupt.

6. (Currently Amended) The microcomputer according to claim 5, wherein said CPU executes a process ~~for changing the~~ that changes a location of an interrupt process routine for a non-maskable interrupt request to an address of a RAM upon execution of the erase and programming.

7. (Currently Amended) A microcomputer comprising:

an erasable and programmable non-volatile memory; and

a CPU,

wherein said non-volatile memory has an erase and program control program executed by said CPU and used for erase/program-controlling of said non-volatile memory,

wherein the erase and program control program allows a process of said CPU to temporarily branch to another ~~branch~~

process for each cycle or plurality of cycles of a unit process for the non-volatile memory, the unit process including the application of an erase voltage for an erase operation or a program voltage for a programming operation, and a verify operation, ~~or every plural cycles~~, and

wherein said CPU specifies said another process according to a value set ~~to~~ in a first register means.

8. (Original) The microcomputer according to claim 7, wherein said first register means is a register selected from general purpose registers of said CPU.

9. (Currently Amended) The microcomputer according to claim 7, further including a RAM disposed in an address space of said CPU, and

wherein said non-volatile memory has a transfer control program ~~for transferring~~ that transfers the erase and program control program to said RAM, and said CPU sets parameters for said another process to the erase and program control program transferred to said RAM, based on the set value of the first register means and thereby executes the erase and program control program.

10. (Original) A microcomputer comprising:

a non-volatile memory including a plurality of electrically programmable memory cells; and

a central processing unit capable of executing a program control program with respect to said non-volatile memory,

wherein said central processing unit is capable of temporarily branching to a process for a first control program different from the program control program during the execution of the program control program.

11. (Currently Amended) The microcomputer according to claim 10,

wherein when information is written into ~~the~~ a specified memory cell of said electrically programmable plural memory cells, the program control program defines a process for executing a plurality ~~of times~~ of program process loops and thereby writing the corresponding information into the specified memory cell, and

wherein the process of said central processing unit is capable of branching to the ~~first~~ control program different from the program control program for ~~said~~ each program process loop.

12. (Currently Amended) The microcomputer according to claim 11, further including a first memory circuit programmable by said central processing unit,

wherein when said first memory circuit is set to a first set value by said central processing unit, the process of said central processing unit continuously executes the program control program, and

wherein when said first memory circuit is set to a second set value different from the first set value by said central processing unit, the process of said central processing unit ~~is branched~~ branches to the ~~first~~ control program different from the program control program ~~for said each program process loop~~.

13. (Original) The microcomputer according to claim 10, wherein each of said plurality of memory cells is an electrically programmable and erasable non-volatile memory cell having a floating gate.

14. (Original) The microcomputer according to claim 10, wherein said non-volatile memory is an electrically programmable and erasable flash memory.

15. (Original) The microcomputer according to claim 10, wherein said non-volatile memory stores the program control program therein.

16. (Original) The microcomputer according to claim 15, further including a memory to which the program control program is transferred from said non-volatile memory.

17. (Original) A microcomputer comprising:

a non-volatile memory including a plurality of electrically erasable memory cells; and

a central processing unit capable of executing an erase control program with respect to said non-volatile memory,

wherein said central processing unit is capable of temporarily branching to a process for a ~~first~~ control program different from the erase control program during the execution of the erase control program.

18. (Currently Amended) The microcomputer according to claim 17,

wherein when information is erased from ~~the~~ a specified memory cell of said electrically erasable plural memory cells, the erase control program defines a process for executing a plurality ~~of times~~ of erase process loops and thereby erasing the corresponding information for the specified memory cell, and

wherein the process of said central processing unit is capable of branching to the ~~first~~ control program different from the erase control program for ~~said~~ each erase process loop.

19. (Currently Amended) The microcomputer according to claim 18, further including a first memory circuit programmable by said central processing unit,

wherein when said first memory circuit is set to a first set value by said central processing unit, the process of said central processing unit continuously executes the erase control program, and

wherein when said first memory circuit is set to a second set value different from the first set value by said central processing unit, the process of said central processing unit ~~is branched~~ branches to the ~~first~~ control

program different from the erase control program ~~for said each erase process loop~~.

20. (Original) The microcomputer according to claim 17, wherein each of said plurality of memory cells is an electrically programmable and erasable non-volatile memory cell having a floating gate.

21. (Original) The microcomputer according to claim 17, wherein said non-volatile memory is an electrically programmable and erasable flash memory.

22. (Original) The microcomputer according to claim 17, wherein said non-volatile memory stores the erase control program therein.

23. (Original) The microcomputer according to claim 22, further including a memory to which the erase control program is transferred from said non-volatile memory.

24. (Original) A microcomputer comprising:

a non-volatile memory including a plurality of electrically erasable and programmable memory cells; and

a central processing unit capable of executing an erase control program and a program control program with respect to said non-volatile memory,

wherein said central processing unit is capable of temporarily branching to a process for a ~~first~~ control program different from the program control program during the execution of the program control program.

25. (Currently Amended) The microcomputer according to claim 24,

wherein when information is written into ~~the~~ a specified memory cell of said electrically erasable and programmable plural memory cells, the program control program defines a process ~~for executing~~ that executes a plurality ~~of times~~ of program process loops and thereby writing the corresponding information into the specified memory cell, and

wherein the process of said central processing unit is capable of branching to the ~~first~~ control program different from the program control program for ~~said~~ each program process loop.

26. (Currently Amended) The microcomputer according to claim 25, further including a first memory circuit programmable by said central processing unit,

wherein when said first memory circuit is set to a first set value by said central processing unit, the process of said central processing unit continuously executes the program control program, and

wherein when said first memory circuit is set to a second set value different from the first set value by said central processing unit, the process of said central processing unit ~~is branched~~ branches to the ~~first~~ control program ~~for said each program process loop~~ different from the program control program.

27. (Original) The microcomputer according to claim 24, wherein each of said plurality of memory cells is a non-volatile memory cell having a floating gate.

28. (Original) The microcomputer according to claim 24, wherein said non-volatile memory is a flash memory.

29. (Original) The microcomputer according to claim 24, wherein said non-volatile memory stores the program control program therein.

30. (Original) The microcomputer according to claim 29, further including a memory to which the program control program is transferred from said non-volatile memory.

31. (Currently Amended) The microcomputer according to claim 26, wherein said central processing unit is capable of temporarily branching to a process for a ~~first~~ control program different from the erase control program during the execution of the erase control program.

32. (Currently Amended) The microcomputer according to claim 31,

wherein when information is erased from ~~the~~ a specified memory cell of said electrically erasable plural memory cells, the erase control program defines a process for executing a plurality of ~~times of~~ erase process loops and thereby erasing the corresponding information for the specified memory cell, and

wherein the process of said central processing unit is capable of branching to the ~~first~~ control program different than the erase control program for said each erase process loop.

33. (Currently Amended) The microcomputer according to claim 32,

wherein when said first memory circuit is set to the first set value by said central processing unit, the process of said central processing unit continuously executes the erase control program, and

wherein when said first memory circuit is set to the second set value by said central processing unit, the process of said central processing unit is branched to the ~~first~~ control program different than the erase control program ~~for said each erase process loop~~.

34. (Currently Amended) A programming method ~~for causing~~ that causes a central processing unit included in a microcomputer having the central processing unit and an electrically programmable non-volatile memory to execute a program control program to thereby write information into said non-volatile memory, comprising:

a first step ~~for~~ of supplying an address for a memory cell to be programmed in the non-volatile memory;

a second step ~~for~~ of supplying information to be programmed to the memory cell; and

a third step ~~for~~ of repeatedly performing a writing operation to write ~~the data~~ information ~~to be programmed~~ into the memory cell,

said ~~third step~~ writing operation including:

a voltage applying step ~~for~~ of applying a program voltage to the memory cell;

a verify step for of ~~for~~ confirming whether the ~~data~~ information to be programmed has been written into the memory cell;

a step ~~for~~ of referring to a value of a predetermined register and transitioning a process of the central processing unit during execution of the third step to a predetermined process corresponding to a predetermined value set to the register when the predetermined value is stored in the register; and

a step ~~for~~ of returning the process of the central processing unit from the predetermined process to said third step.

35. (Currently Amended) An erasing method ~~for causing~~ that causes a central processing unit included in a microcomputer having the central processing unit and an electrically erasable non-volatile memory to execute an erase program to thereby erase information stored in a predetermined memory cell of said non-volatile memory, comprising:

a first step ~~for~~ of supplying an address for a memory cell to be erased in the non-volatile memory; and

a second step ~~for~~ of erasing the information from the memory cell,

said second step including:

a voltage applying step ~~for~~ of applying an erase voltage to the memory cell;

a verify step ~~for~~ of confirming whether the information has been erased from the memory cell;

a step ~~for~~ of referring to a value of a predetermined register and transitioning a process of the central processing unit during execution of the second step to a predetermined process corresponding to a predetermined value set ~~to~~ in the register when the predetermined value is stored in the register; and

a step ~~for~~ of returning the process of the central processing unit from the predetermined process to said second step.

36. (Currently Amended) A programming method ~~for mounting~~ that mounts a microcomputer having a central processing unit and an electrically programmable non-volatile memory ~~to a substrate~~ and thereafter ~~causing~~ causes the central processing unit to execute a program control program to thereby write information into a predetermined memory cell of said non-volatile memory, comprising:

a first step ~~for~~ of supplying an address for a memory cell to be programmed in the non-volatile memory;

a second step ~~for~~ of supplying information to be programmed to the memory cell; and

a third step ~~for~~ of repeatedly performing a writing operation to write information ~~the data to be programmed~~ into the memory cell,

said third step including:

a voltage applying step ~~for~~ of applying a program voltage to the memory cell;

a verify step ~~for~~ of confirming whether the data to be programmed has been written into the memory cell;

a step ~~for~~ of causing the process of the central processing unit to transit during execution of the third step to a predetermined process; and

a step ~~for~~ of returning the process of the central processing unit from the predetermined process to said third step.

37. (Currently Amended) The programming method according to claim 36, wherein said step ~~for~~ of causing the process of the central processing unit to transit to the predetermined process includes a step ~~for~~ of referring to a value of a predetermined register and allowing the process thereof to transit to the predetermined process corresponding to the value set ~~to~~ in the register ~~where the predetermined value is stored in the register~~.

38. (Currently Amended) An erasing method ~~for mounting~~ that mounts a microcomputer having a central processing unit and an electrically erasable non-volatile memory ~~to a substrate~~ and thereafter ~~causing~~ causes the central processing unit to execute an erase program to

thereby erase information stored in a predetermined memory cell of said non-volatile memory, comprising:

a first step ~~for~~ of supplying an address for a memory cell to be erased in the non-volatile memory; and

a second step ~~for~~ of erasing the information from the memory cell,

said second step including:

a voltage applying step ~~for~~ of applying an erase voltage to the memory cell;

a verify step ~~for~~ of confirming whether the information has been erased from the memory cell;

a step ~~for~~ of causing the process of the central processing unit to transit during execution of the second step to a predetermined process; and

a step ~~for~~ of returning the process of the central processing unit from the predetermined process to said second step.

39. (Currently Amended) The erasing method according to claim 38, wherein said step ~~for~~ of causing the process of the central processing unit to transit to the predetermined process includes a step ~~for~~ of referring to a value of a predetermined register and allowing the process

thereof to transit to the predetermined process corresponding to the value set ~~to~~ in the register ~~where the predetermined value is stored in the register~~.

40. (Currently Amended) The microcomputer according to claim 2, further including second register means (FKEY) readable and writable by said CPU, and

wherein said non-volatile memory sets ~~the setting of~~ a second set value ~~to~~ in said second register means as a necessary condition for enabling erase and programming operations, and

said CPU sets a value other than the second set value ~~to~~ in said second register means upon said branch and ~~sets~~ resets the second set value to said second register means for each return from the branch.

41. (Previously Presented) The microcomputer according to claim 40, wherein the value other than the second set value is code information indicative of the progress of an erase and program process.

42. (Currently Amended) The microcomputer according to claim 2, further including an interrupt control circuit

~~for inputting~~ that inputs an interrupt request signal therein, and ~~performing~~ performs arbitration of interrupt requests which compete with one another, and an interrupt priority level-based interrupt mask process to thereby output an interrupt signal to said CPU, and

wherein said CPU causes said interrupt control circuit to carry out a setting for masking an interrupt lower in interrupt priority level than a non-maskable interrupt.

43. (Currently Amended) The microcomputer according to claim 42, wherein said CPU executes a process ~~for changing the~~ that changes a location of an interrupt process routine for a non-maskable interrupt request to an address of a RAM upon execution of the erase and programming.

44. (Currently Amended) The microcomputer according to claim 8, further including a RAM disposed in an address space of said CPU, and

wherein said non-volatile memory has a transfer control program ~~for transferring~~ that transfers the erase and program control program to said RAM, and said CPU sets parameters for said another process to the erase and

program control program transferred to said RAM, based on the set value of the first register means and thereby executes the erase and program control program.